Remarks

Entry of the Amendments presented, and reconsideration and withdrawal of the specification objection and claim rejections are respectfully requested. With entrance of this Amendment, claims 15-21 are pending.

By this paper, non-elected claims 1-5 are canceled herein without prejudice to the re-filing thereof in a further divisional application. Further, claims 6-14 are canceled without prejudice in favor of new, rewritten claims 15-21. New claims 15-21 are supported throughout the specification. For example, reference FIGS. 2 & 5-10b, as well as their supporting discussion in the specification. In accordance with the specification amendments presented herewith, Applicants provide further explanation for their use of "first contact hole" and "second contact hole" in the new claims. By way of further explanation, in one embodiment, the recited first conductive material could comprise polysilicon gate (108), and the second conductive material might comprise a bit-line polysilicon contact (134) (see FIG. 10b), while the electrically insulating spacer lining at least a portion of the second contact hole could comprise spacers (150) & (160). In view of this, no new matter is added to the application by any amendment presented.

Based upon the cancellations of claim 6-14, withdrawal of the specification objection and the 35 U.S.C. §112 rejection to claims 10, 11 & 13 is respectfully requested.

Substantively, claims 6-10 and 12-14 were rejected under 35 U.S.C. §102(e) as being anticipated by Kinoshita et al. (U.S. Patent No. 6,271,087; hereinafter Kinoshita), while claims 6 & 9-11 were rejected under 35 U.S.C. §102(e) as being anticipated by Nesbit et al. (U.S. Patent No. 6,686,668; hereinafter Nesbit). Each of these rejections is respectfully, but most strenuously, traversed to any extent deemed applicable to claims 15-21 presented herewith.

Independent claim 15 more particularly recites Applicants' semiconductor processing method wherein a first conductive material is provided above a substrate, with a first contact hole being disposed adjacent to the first conductive material and a horizontal surface of the first conductive material being disposed adjacent to the first contact hole. The method further includes providing a mask extending over a portion of the first conductive material, with the mask having a second contact hole formed therein which extends over the first contact hole and

exposes a portion of the first horizontal surface of the first conductive material. Next, a second conductive material is disposed in the first contact hole, and thereafter an electrically insulating spacer is provided lining at least a portion of the section contact hole and extending to the second conductive material. The insulating spacer has a dimension sufficient so that the horizontal surface of the first conductive material is unexposed, and the second conductive material is recessed below the horizontal surface of the first conductive material.

It is well settled that there is no anticipation of a claim unless a single prior art reference discloses: (1) all the same elements of the claimed invention; (2) found in the same situation as the claimed invention; (3) united in the same way as the claimed; and (4) in order to perform the identical function as the claimed invention. In this instance, Kinoshita and Nesbit each fail to disclose certain aspects of Applicants' semiconductor processing method as recited in claim 15, as well as various dependent claims, and as a result, does not anticipate (or even render obvious) Applicants' invention.

Kinoshita discloses in Figs. 3A-3E a conventional sequence of process steps for forming core and peripheral contacts for a memory device. A gate film 224 is exposed in Fig. 3c via a hole 235 so that a portion of the top surface of gate film 224 is exposed. A material 239 is then provided filing hole 235 (Fig. 3D). This material is removed above the dielectric layer 232 to form the peripheral local interconnect 241 electrically contacting both gate film 224 and source region 202c (Fig. 3E).

In stating the initial rejection to Applicants' claim 6, the Office Action alleged at the top of page 5:

> The material deposited into the "hole" correlates to the region of material (239) that is formed between the substrate and the top layer (224), and the spacer is the region of material (239) from the top of (224) to the top of (232) and above.

This characterization of the teachings of Kinoshita is respectfully, but most strenuously, traversed to any extent deemed applicable to claim 15. As noted above, Applicants recite providing an electrically insulating spacer lining at least a portion of the second contact hole and extending to the second conductive material. This electrically insulating spacer has a dimension sufficient so that the first conductive material is unexposed, and the second conductive material

is recessed below the horizontal surface of the first conductive material. Clearly, second conductive material 239/241 of Figs. 3D & 3E in Kinoshita electrically contacts with first conductive material 224, and therefore, the processing described therein does not anticipate, or even render obvious, Applicants' recited invention. Further, there would be no teaching or suggestion in the art for further modifying Kinoshita since the purpose of contact 241 is to provide a common electrical connection to both the gate film and the source diffusion.

For the above reasons, Applicants respectfully submit that independent claim 15 patentably distinguishes over the teachings of Kinoshita.

Nesbit depicts in Figs. 2 & 5-9 a semiconductor processing method wherein a substrate has multiple gate conductors including polysilicon layer 10, a WSi_x (or W/Wn) layer 15, and an Si_3N_4 insulating layer 20 formed over the WSi_x layer 15 and the sidewalls of both the polysilicon layer 10 and the WSi_x layer 15. This insulating material 20 may also be an oxidation as well as silicon nitride. In Fig. 6, at least a portion of insulating layer 20 of each gate conductor is exposed and a low pressure chemical vapor deposition N+ amorphous/polycrystalline silicon layer 45 is deposited (see Fig. 7). This layer is then etched below the capping nitride layer 20 as shown in Fig. 8 and a bit-line (M0) TEOS layer 50 is deposited thereon.

Applicants respectfully submit that numerous aspects of their semiconductor processing method as recited in claim 15 are simply not taught or suggested by the processing approach of Nesbit. For example, Applicants recite providing a first conductive material above a substrate with a first contact hole being disposed adjacent to the first conductive material and a horizontal surface of the first conductive material adjacent to the first contact hole. In Applicants' process, a mask is extended over a portion of the first conductive material and the mask has a second contact hole formed therein. The second contact hole extends over the first contact hole and exposes a portion of the horizontal surface of the first conductive material. In this respect, Applicants note that layer 20 in Nesbit is an insulating layer, and the conductive film protected by the insulating layer is never exposed.

After disposing a second conductive material in the first contact hole, Applicants further recite providing an electrically insulating spacer lining at least a portion of the second contact hole and extending to the second conductive material. This electrically insulating spacer has a dimension sufficient so that the first conductive material is unexposed, and the second conductive material is recessed below the first conductive material. Clearly, since the conductive material within the gate stack of Nesbit is never exposed, there is no need for providing a further electrical insulating spacer lining at least a portion of a second contact hole and extending to the second conductive material. In accordance with Applicants' invention, the first conductive material remains relatively exposed, to allow access to provide electrodes to the diffusion implants (i.e., via the first contact hole and the second conductive material disposed therein).

In view of the above, Applicants respectfully submit that the processing of Nesbit does not anticipate, or even render obvious, Applicants' particular semiconductor processing method recited in new independent claim 15.

The dependent claims are a believed allowable for the same reasons as the independent claim, as well as for their own additional characterizations. For example, claim 21 recites that the providing of the electrically insulating spacer includes, in part, creating an insulating layer aligned to the second contact hole and extending into the first conductive material and the second conductive material. No similar processing is described in the applied art.

For the above reasons, Applicants respectfully submit that all claims are in condition for allowance, and such action is respectfully requested.

Applicants' undersigned attorney is available should the Examiner wish to discuss this application further.

Respectfully submitted,

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